

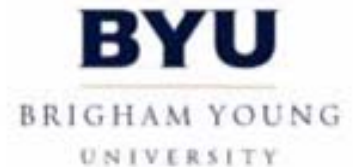
FPGA Design Productivity

Brent Nelson

NSF Center for High-Performance Reconfigurable
Computing (CHREC)

and

Brigham Young University

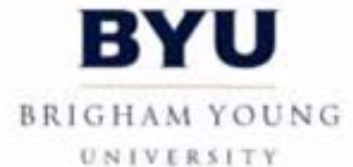


or...

Why Is He Talking About FPGA Design Productivity at an Applied RC Conference?

Brent Nelson

NSF Center for High-Performance Reconfigurable Computing (CHREC)
and
Brigham Young University



Some Terminology

- RTR
 - Run-Time Reconfiguration
 - Reconfiguration at the *cycle* level
- CTR
 - Compile-Time Reconfiguration
 - Reconfiguration at the *application* level
- ASIC Replacement
 - No reconfiguration

CTR

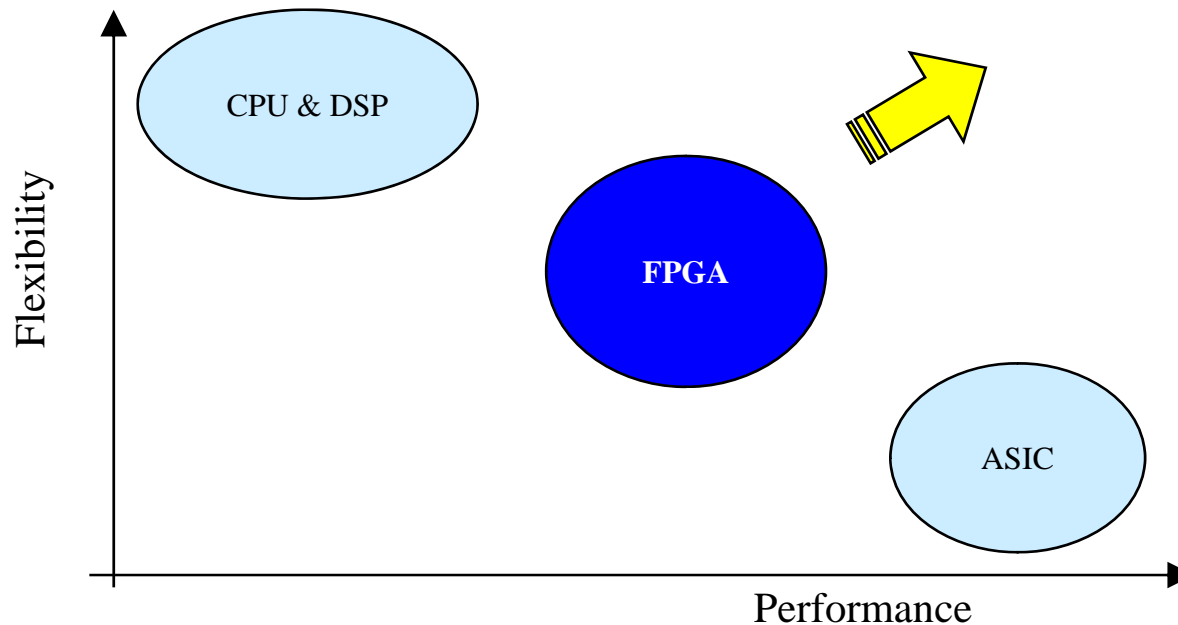
- Use of standard:

- Platforms
- Runtime
- Debug
- IO support

Rapid development
Reuse

- Embedded - yes HPC - ?¹

Configurable Computing Machines (CCM's) circa 1995



All the power of ASICs with all the flexibility of CPUs...

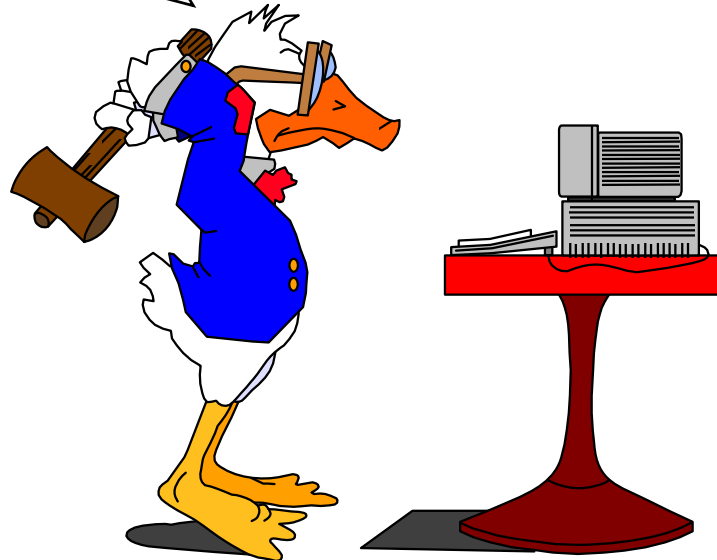
FPGA Apps circa 1995

- ① Small data objects
- ② Modest arithmetic
- ③ Data-parallelism
- ④ Pipeline-ability
- ⑤ Simple control

→ DSP
Comm

Fast Forward 14+ Years...

Excuse me for a minute while I
reconfigure ...



FPGA Apps circa 2009

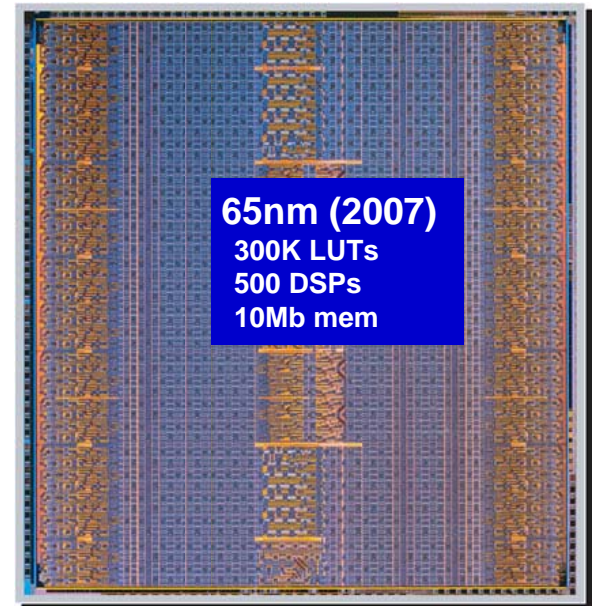
- ① Small data objects
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- ③ Data-parallelism
- ④ Pipeline-ability
- ⑤ Simple control



What has changed?

FPGAs Have Changed

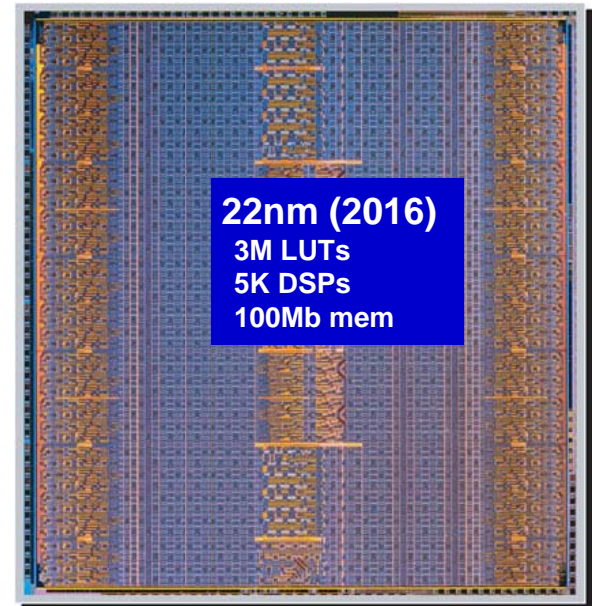
- Bigger, faster
- Increasing custom silicon content
 - Multipliers/DSP blocks
 - Memories
 - CPUs
 - I/O



FPGAs Have Changed

- Bigger, faster
- Increasing custom silicon content
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And they will continue to change...



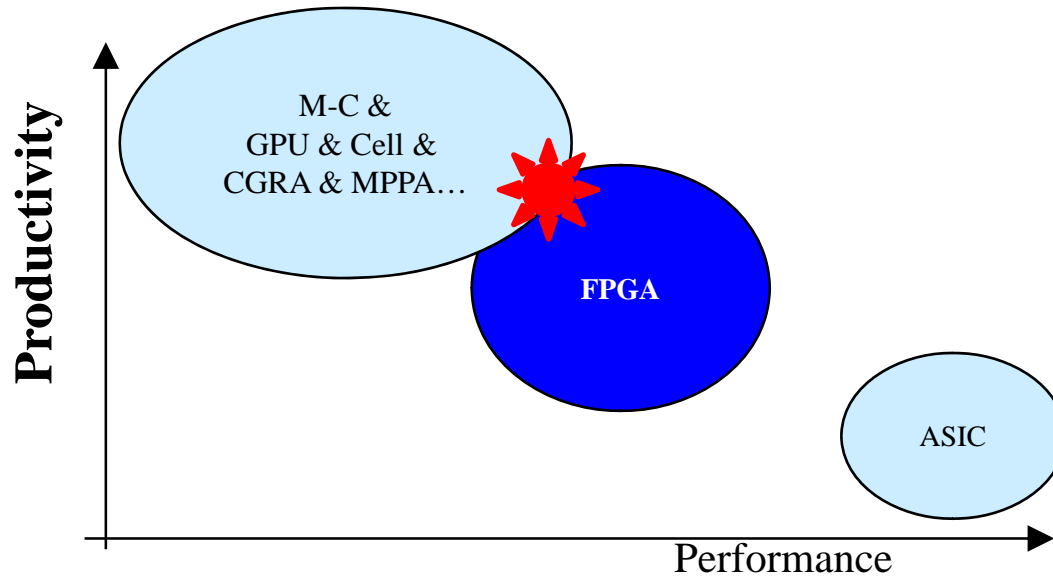
The World is Changing Too...

HW: The Athanas List

- 3P plus 1 Technology
- Achronix Semiconductor Corp
- Ambric
- Ascenium Corp
- Aspex
- ChipWrights
- Clearspeed
- Coherent Logix
- Connex
- Context Corporation
- Cradle
- Element CXI
- IP Flex
- Icera Semiconductor Ltd
- Ikoa Corporation
- Intelliasys Corporation
- M2000
- MathStar
- Mesh Semiconductor
- Morphotech
- PACT
- Picochip Designs
- Pluarity
- Rapport
- Raytheon Monarch
- ReCore
- Sandbridge
- Silicon Hive
- Spiral Gateway
- Stream Processors
- Stretch
- Systemonic
- Tabula
- Tileria
- Videantis
- Vivace Semiconductor
- XMOS Semiconductor
- Xelerated

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CCM's circa 2009



Some Things Haven't Changed...

- FPGA design ↔ hardware design (still)
 - Manual scheduling & resource sharing
 - Manual memory management
- CAD is still an issue, HDL's still dominate

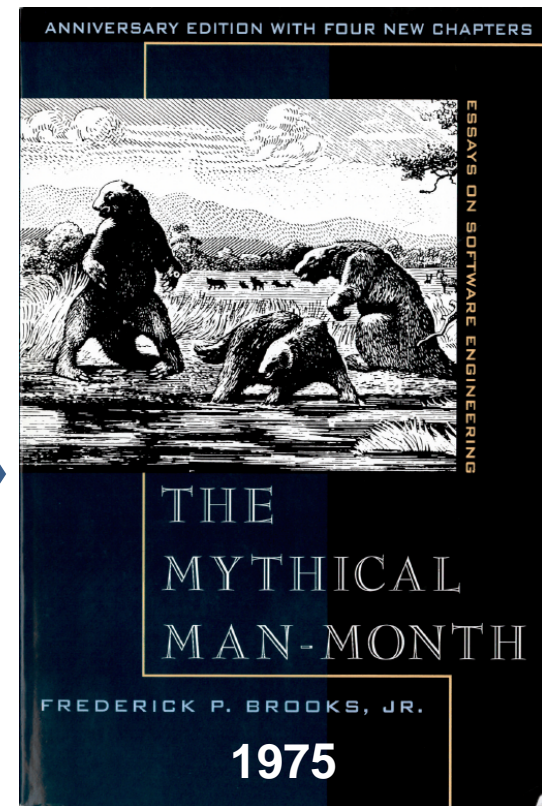


Design Productivity: Where Are We?

- Low-level languages -> higher level languages
- Simple data structures
- Custom design of many (most?) details:
 - Memory allocation
 - Control structures
- Simulation: key development technique
- Debug: batch mode, tracing, value dumps
 - > 50% development time
- Focus on size

Design Productivity: Where Are We?

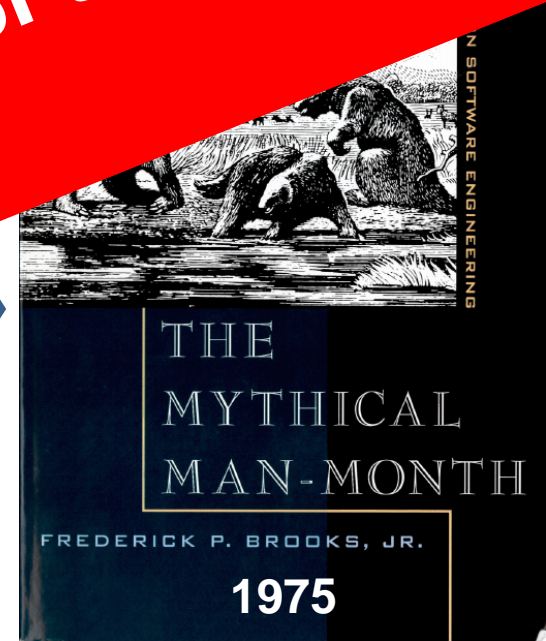
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Design Productivity: Where Are We?

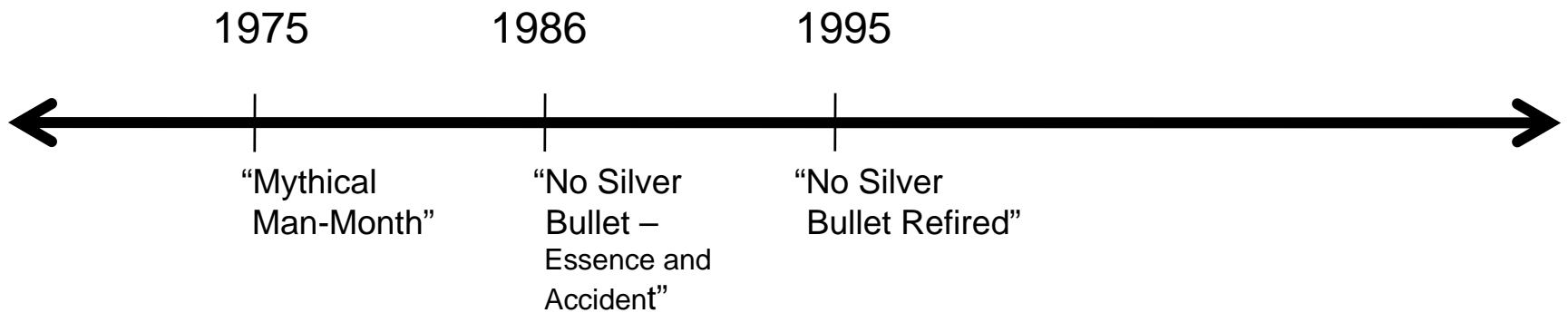
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- Simple data structures
- Custom design
 - Memory
 - ...
- ...
- Focus on size

Software Development of the 1960's

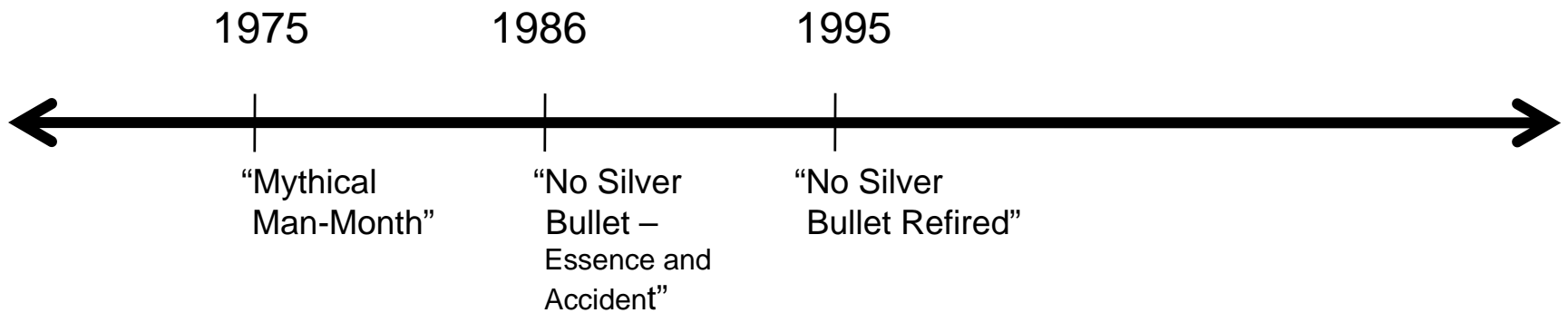


Is A 10X Productivity Improvement Feasible?

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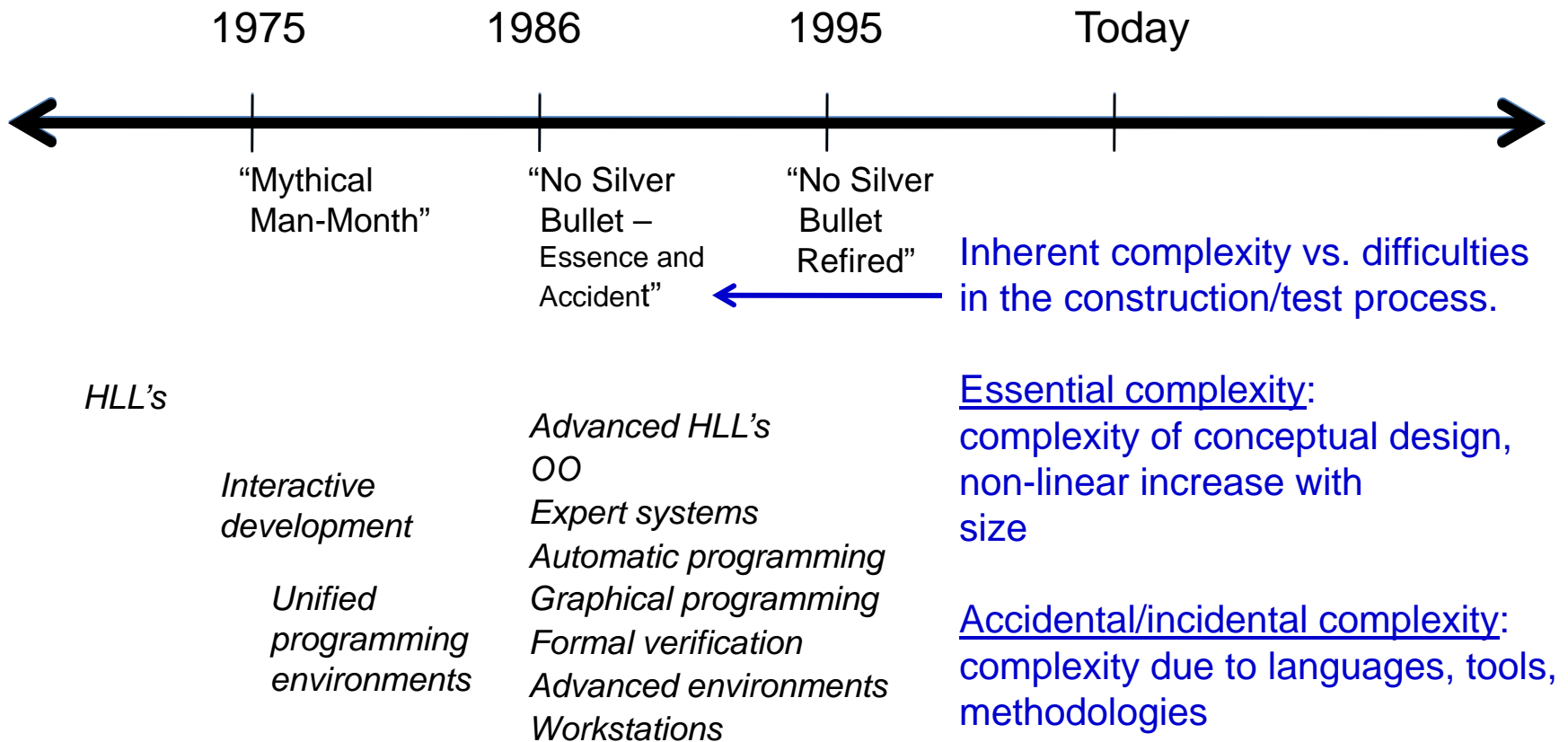


HLL's (5x)

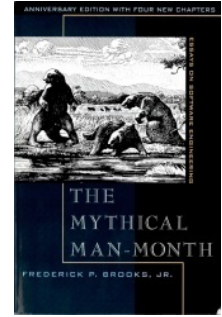
Interactive development (2x)

Unified programming environments ("Integral factors")

Is A 10X Productivity Improvement Feasible?

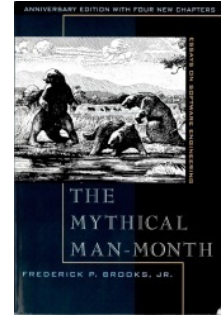


Initial Roots of SW Productivity: High Level Languages



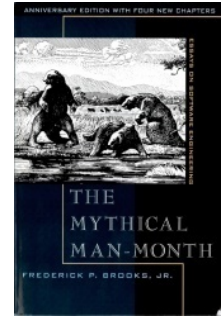
- “5x productivity boost”
- Frees programmer from layers of accidental complexities: register allocation, control flow, procedure call stack frames
- “The most a high-level language can do is furnish all the constructs the programmer imagines in the abstract program.”

Initial Roots of SW Productivity: Interactive Development



- “2x productivity boost”
- “Slow turnaround means we *forget the minutiae*, if not the very thrust of what we were thinking.”
- “The most serious effect may well be the *decay of grasp* of all that is going on in a complex system.”
- “Preserves *immediacy*, and hence enables us to maintain an overview of complexity.”

Initial Roots of SW Productivity: Unified Environments



- “Integral factors of productivity boost”
- “They attack the accidental difficulties of *using programs together* by providing integrated *libraries*, file formats,”
- “As a result, conceptual structures that *in principle* could always call, feed, and use one another can indeed easily do so *in practice*.”



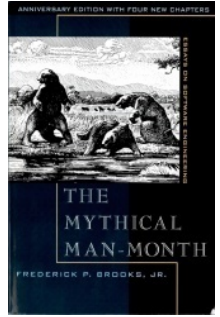
What does this mean for RC?



What does this mean for RC?

- HLL's (**Abstraction**)
- + Interactive Development (**Turns Per Day**)
- + Unified Environments (**Reuse**)

An Excess of Riches...



- "O/S's,

loudly decried in the 1960's for their memory/cycle costs,

have turned to be a good use for our abundant MIPs."

"No Silver Bullet", IFIPS Conference, 1986.



What could we spend
our abundant silicon on?

HW: The Athanas List

- 3P plus 1 Technology
- Achronix Semiconductor Corp
- Ambric
- Ascenium Corp
- Aspex
- ChipWrights
- Clearspeed
- Coherent Logix
- Connex
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- Systemonic
- Tabula
- Tiler
- Videantis
- Vivace Semiconductor
- XMOS Semiconductor
- Xelerated

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HLL & CAD: The Wirthlin List

- AcceIDSP
- Agility Compiler
- AutoESL
- AutoPilot
- BinaChip-FPGA
- Bluespec SystemC
- Bluespec SystemVerilog
- C2H
- C2R
- Carte
- Cascade CoProcessor
- CatapultC
- Computational Adrenaline
- CoreFire
- Cynthesizer
- DSP Builder
- Dime-C
- Handel-C
- Filter Design HDL Coder
- Hyper Streams
- ImpulseC
- LabView FPGA
- MitrionC
- Mobius
- Pico Express
- Pixel Streams
- Simulink HDL Coder
- Stone Ridge Compiler
- SynplifyDSP
- System Generator
- Viva

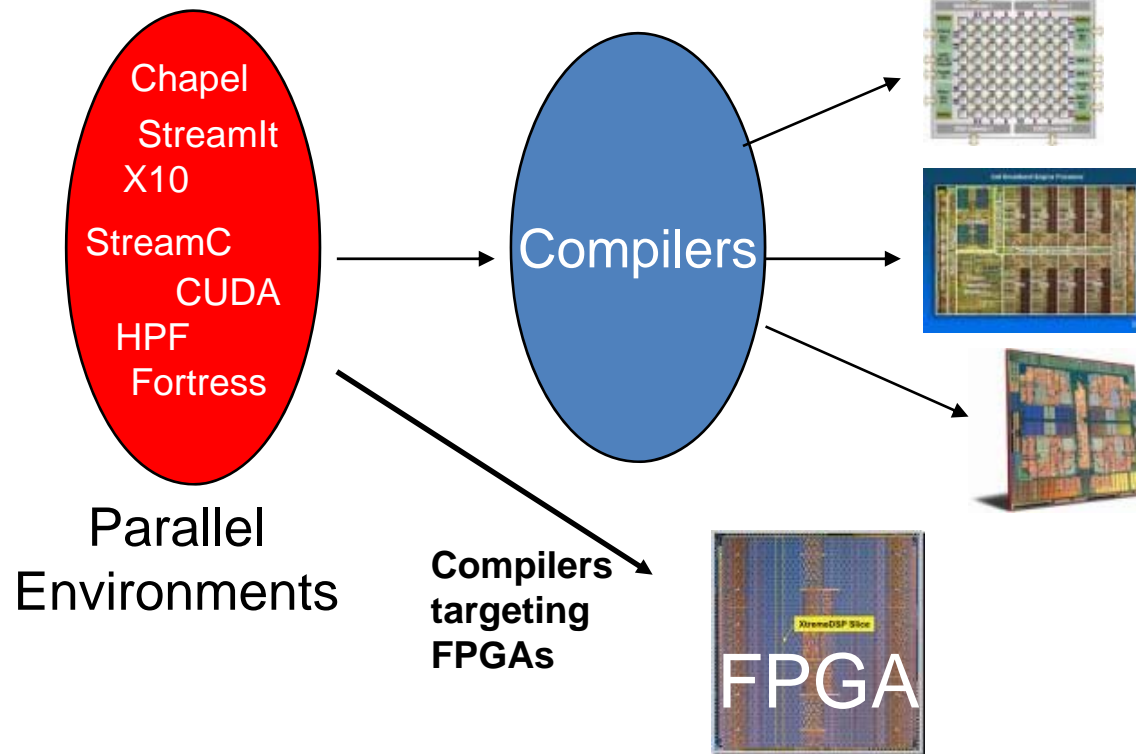
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Challenges & Opportunities:

- Every HLL tool ⇔
 - A new model of computation

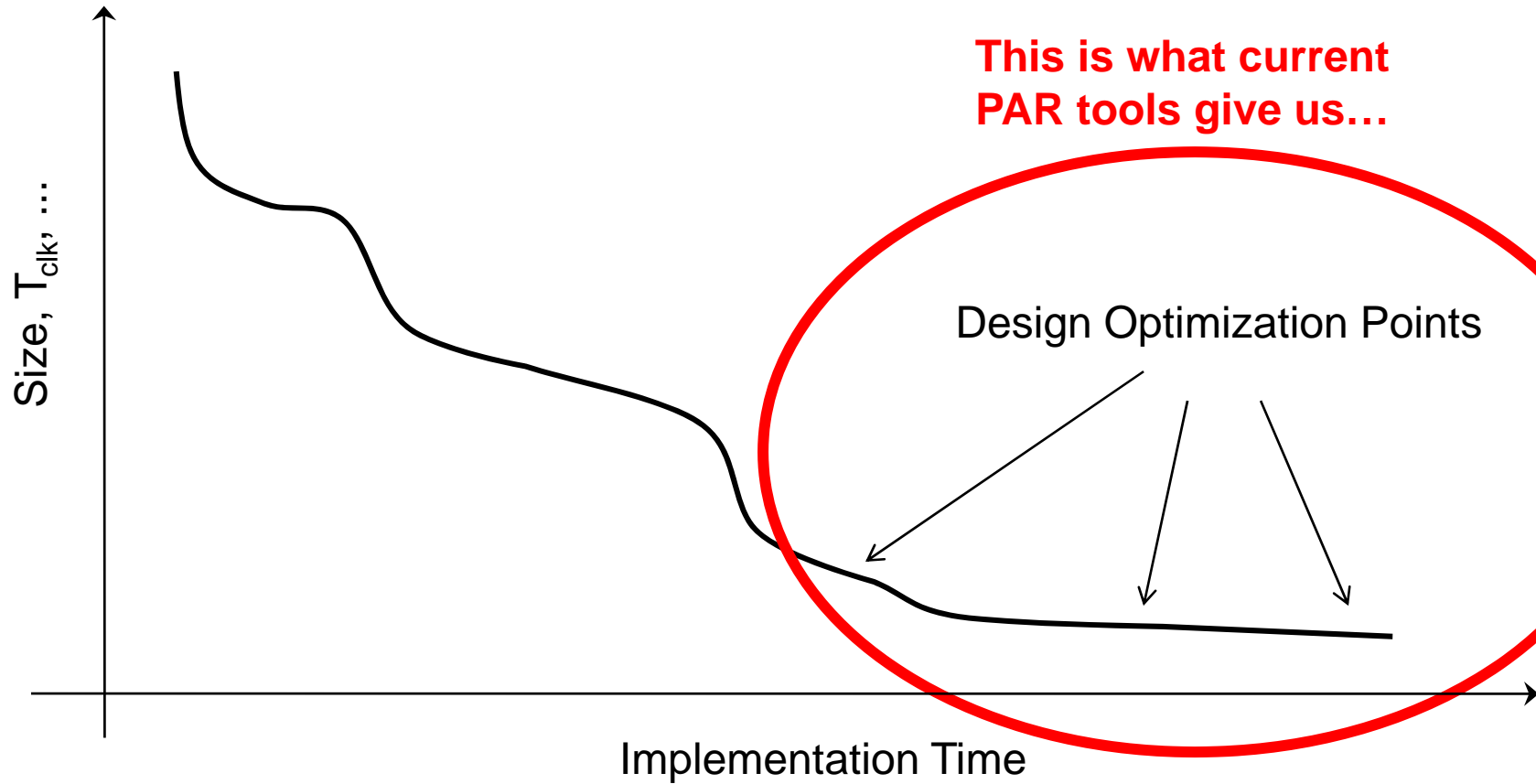
- An opportunity
 - Which ones work? Which ones don't?
 - Which ones imply HW architecture?
 - What app areas are implied?

Parallel HLL's

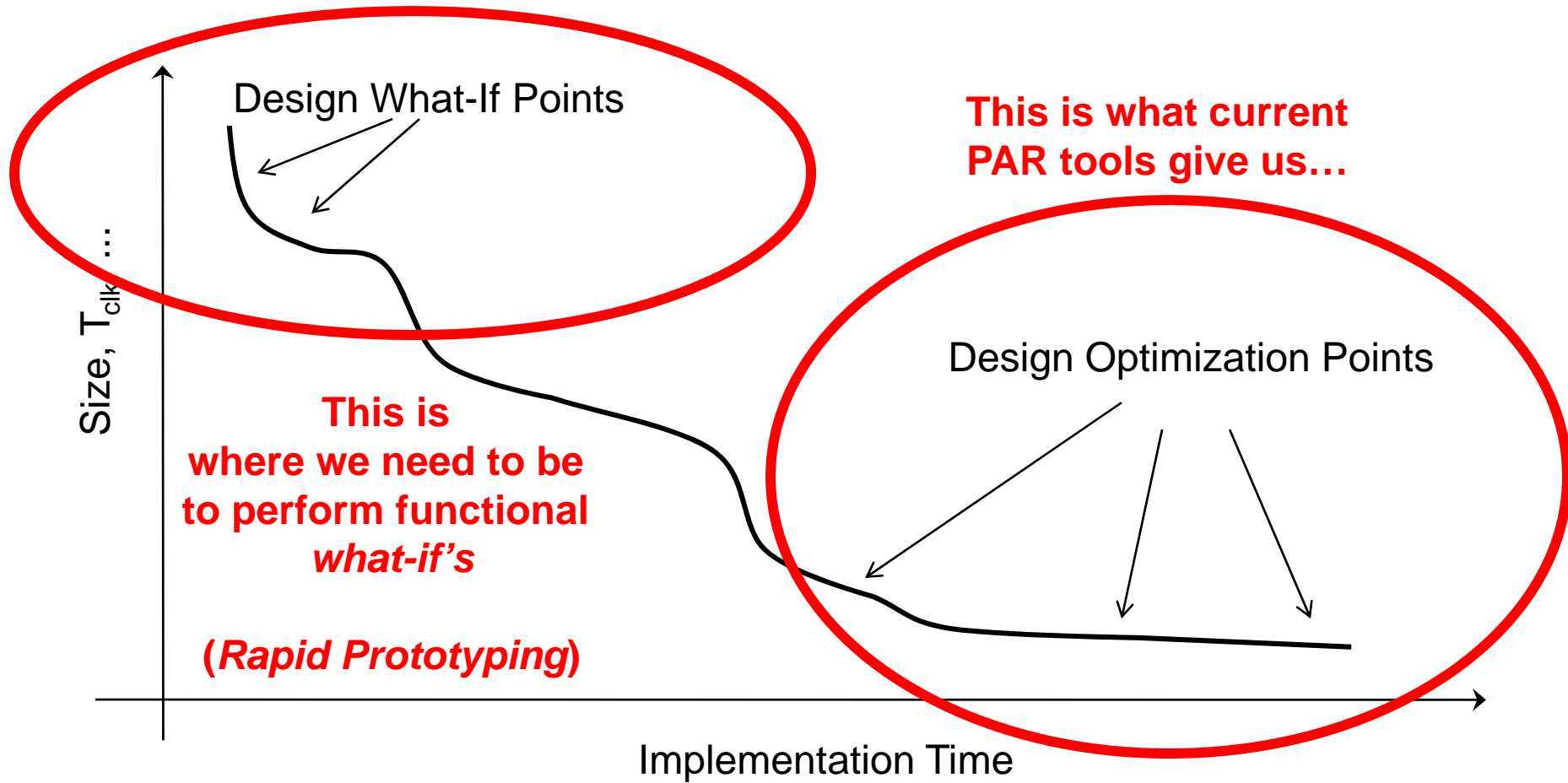


- Can we leverage current investments in parallel programming?

Exploratory Design

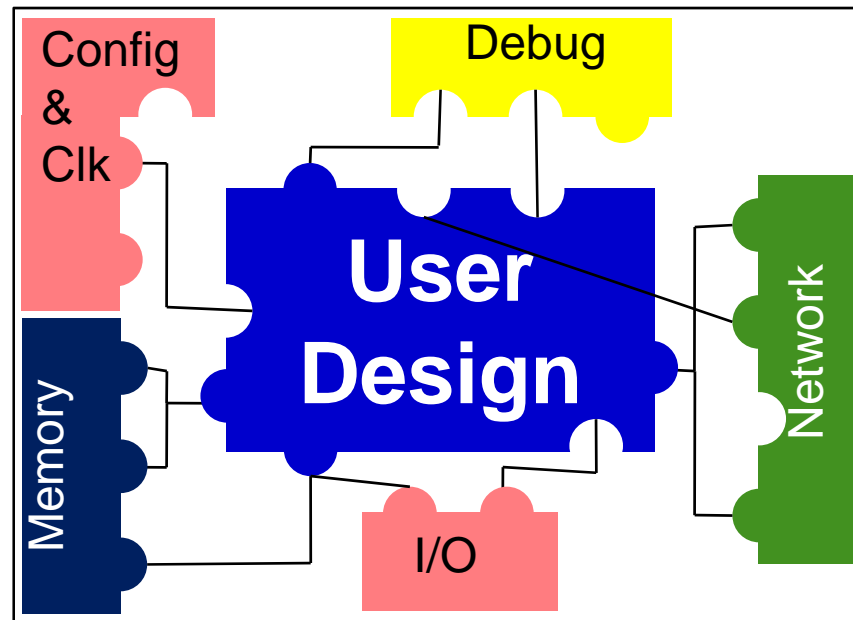


Exploratory Design



Firmware & Incremental Design

- Pre-placed/routed macros
- Incremental compilation

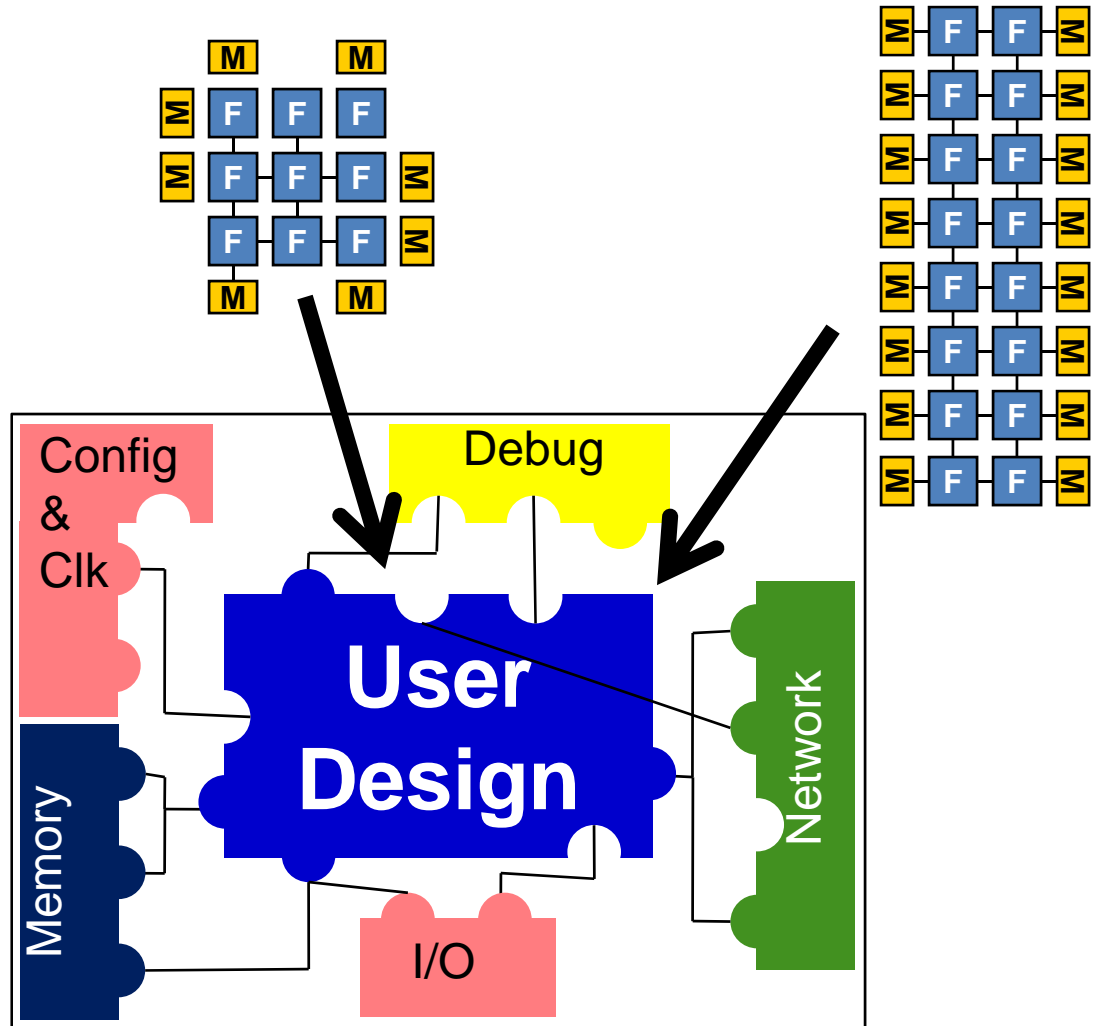


Firmware & Incremental Design

(1) *Compiler/synthesizer/PAR selects required service modules based on user design*

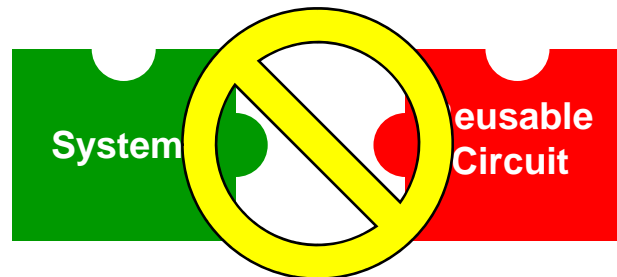
(2) *Compiler/synthesizer/PAR integrates user design with service modules.*

(3) *User focuses only on the Computations, **not** the machine design itself...*

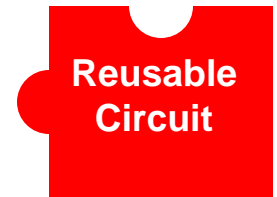
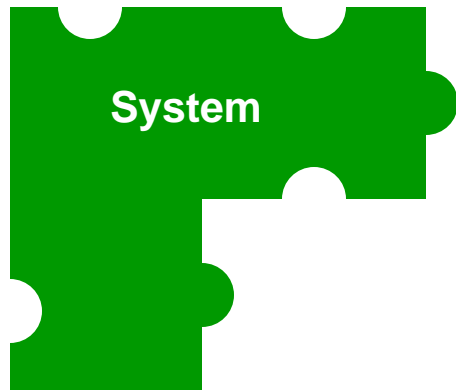


Interface Synthesis

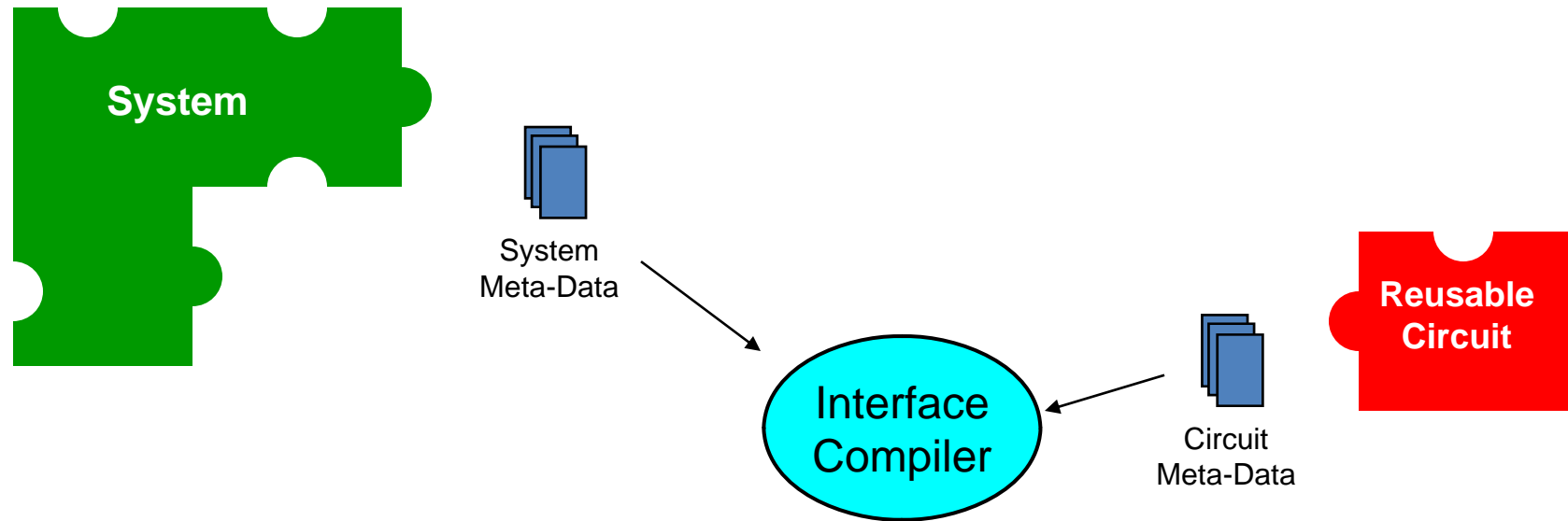
- To reuse FPGA circuits you must:
 - select
 - understand
 - interface
 - verify the custom circuits
- No reuse if $> 30\%$ original effort



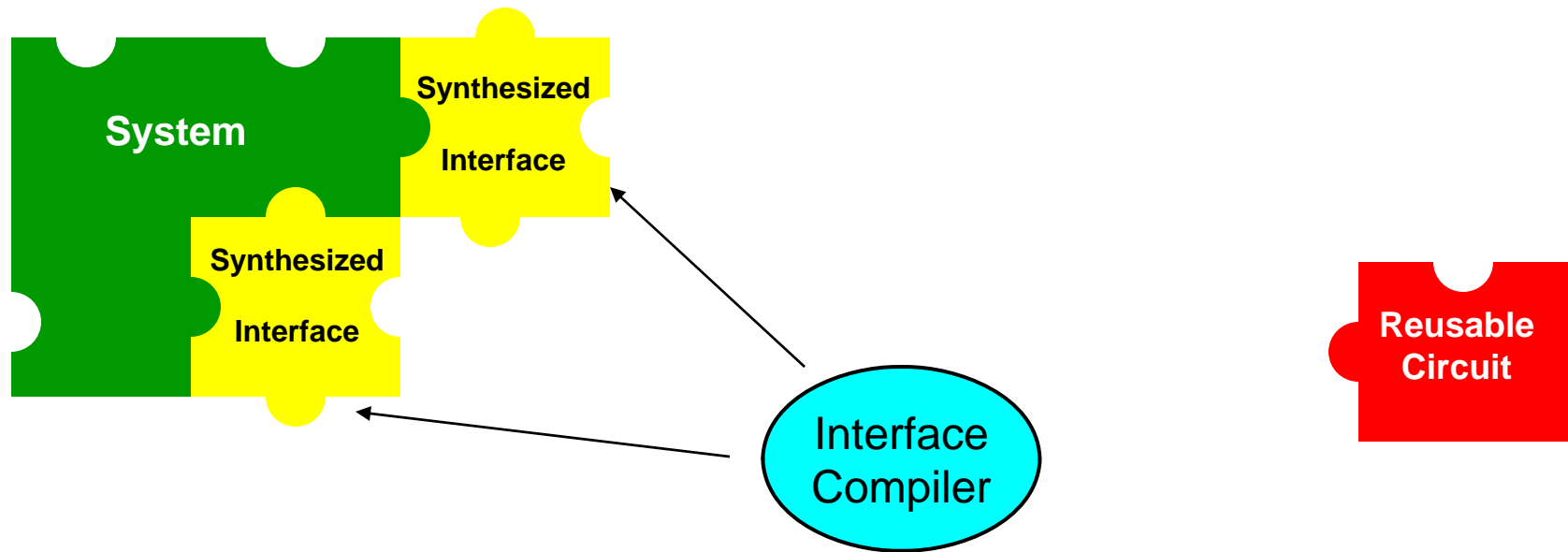
Interface Synthesis



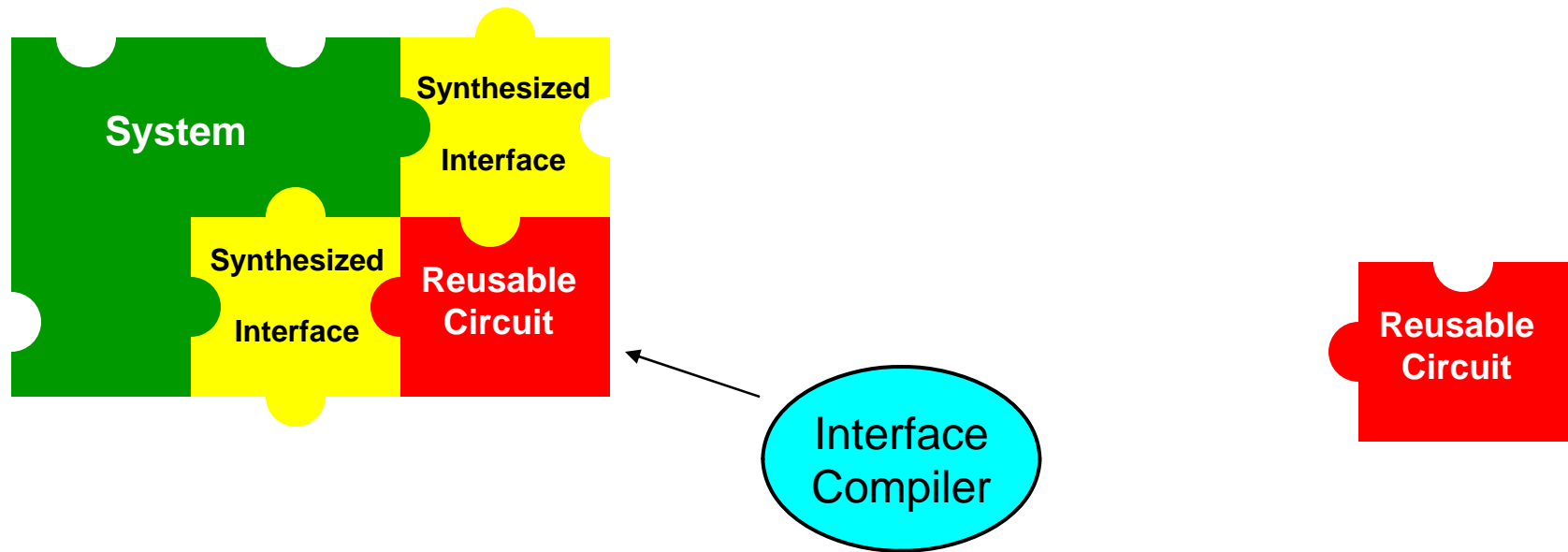
Interface Synthesis



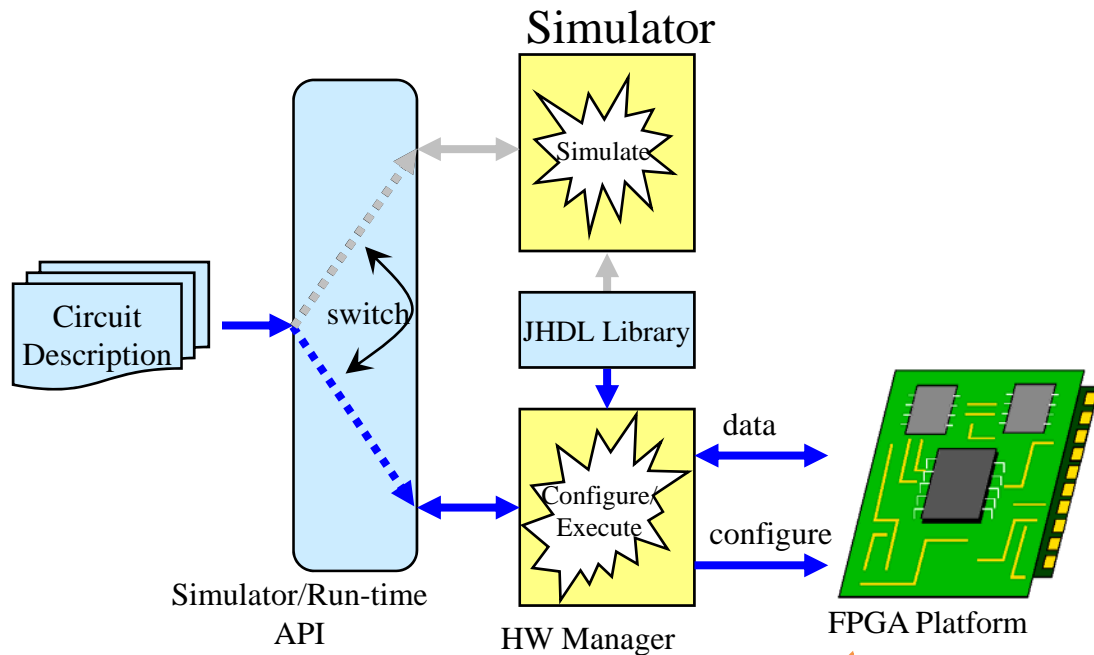
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Interface Synthesis

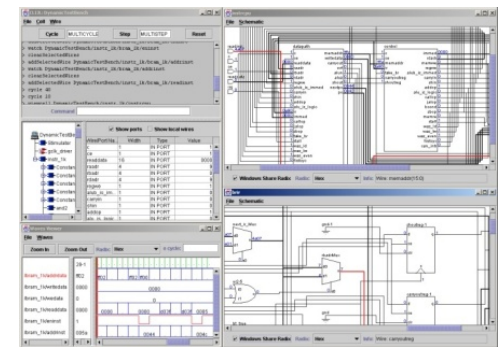


Advanced Debug

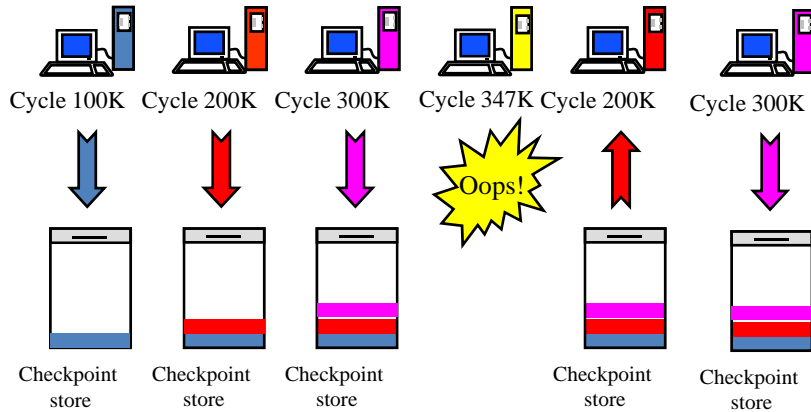


Platform has built-in support circuits for debug...

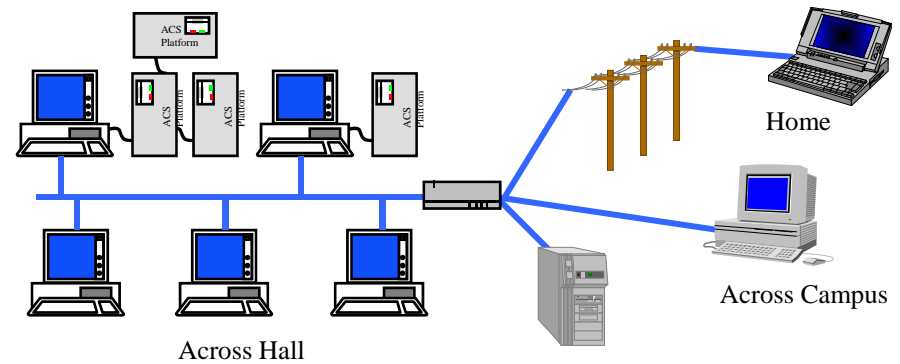
- Example: **JHDL System**
 - Source level debug
 - Debug instrumentation
 - Bitstream mod for rapid *what-if*
 - Full platform support provided...



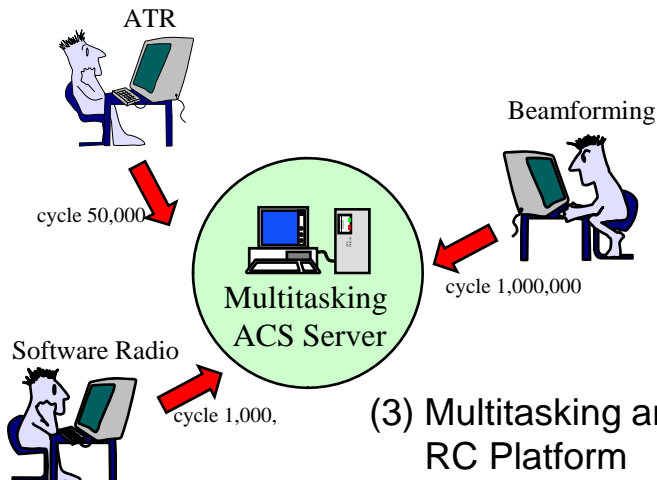
Advanced Debug Concepts



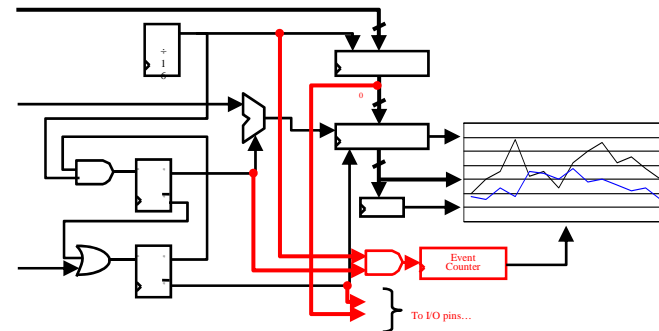
(1) Hardware Checkpointing



(2) Remote Access/Control/Debug of RC Platform

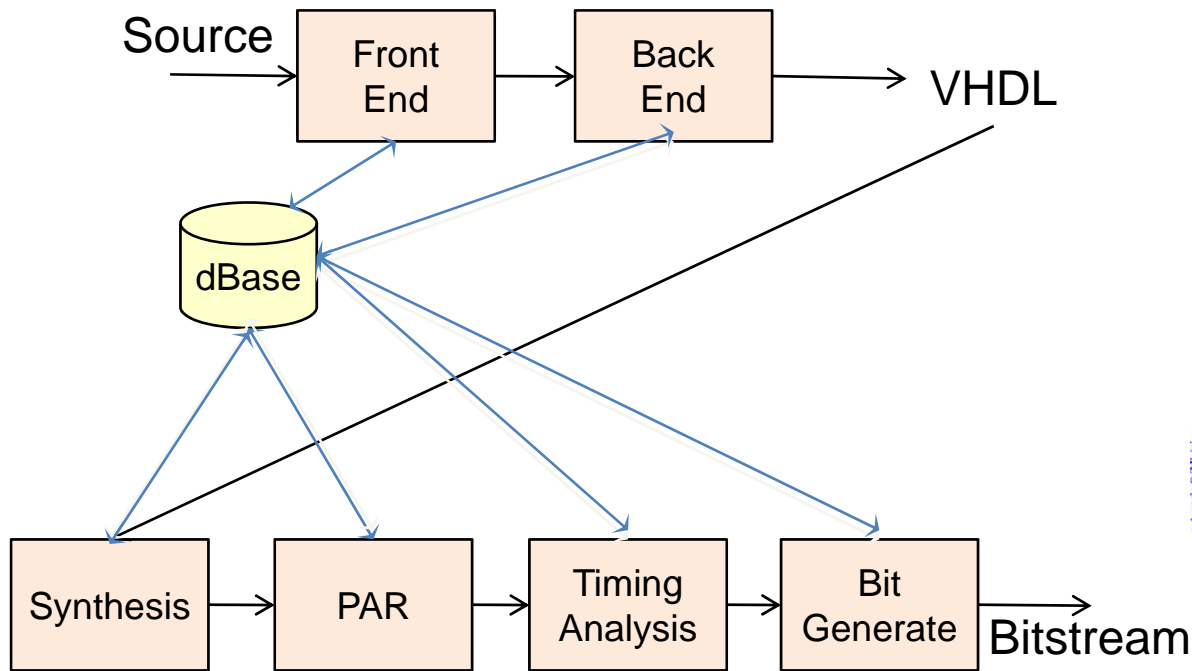


(3) Multitasking an RC Platform



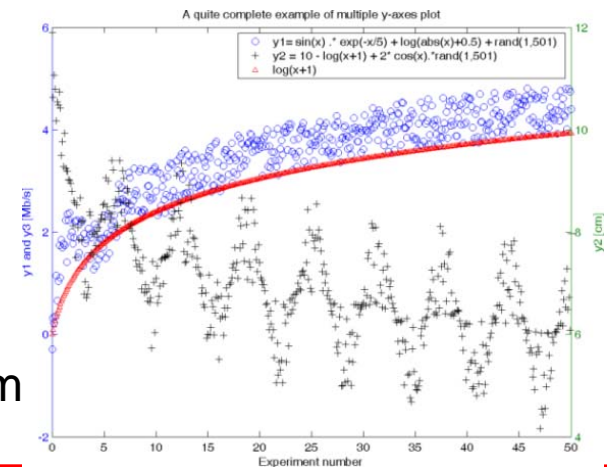
(4) On-the-fly Debug Circuitry Synthesis and Instrumentation

High-Level Abstraction Debug



```

test: Breakfast.java
20; index++) {
49:   int index = 0;
50:   while ( index < 20 ) {
51:     //   int c = 5;
52:     if ( (index & 1) == 0 ) {
53:       even += index;
54:     //   even = index;
55:     }
56:     else {
57:       odd += index;
58:     //   even = c; index = 10;
59:     }
60:     total += index;
61:     index++;
62:   }
  
```



Other Approaches

- POLR (Plain Old Library Reuse)
- Leveraged libraries in selected domains
- Advanced debug for interactive dev.
- Design patterns
- Architecture hooks
- Corba-like reuse
- Two-level compilation for retargeting
- ...

Summarizing...

Three Major Points

Three Major Points

1. Be optimistic

- HLL & parallel development going on

Three Major Points

1. Be optimistic

- HLL & parallel development going on

2. Be optimistic

- Wealth of new HW devices

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1. Be optimistic

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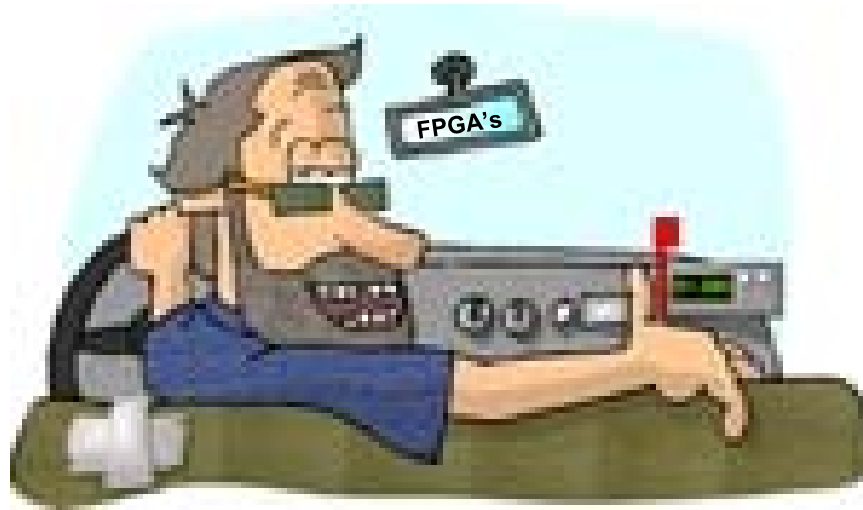
3. Be optimistic

- On the cusp of a 10-20x productivity boost?

Keys

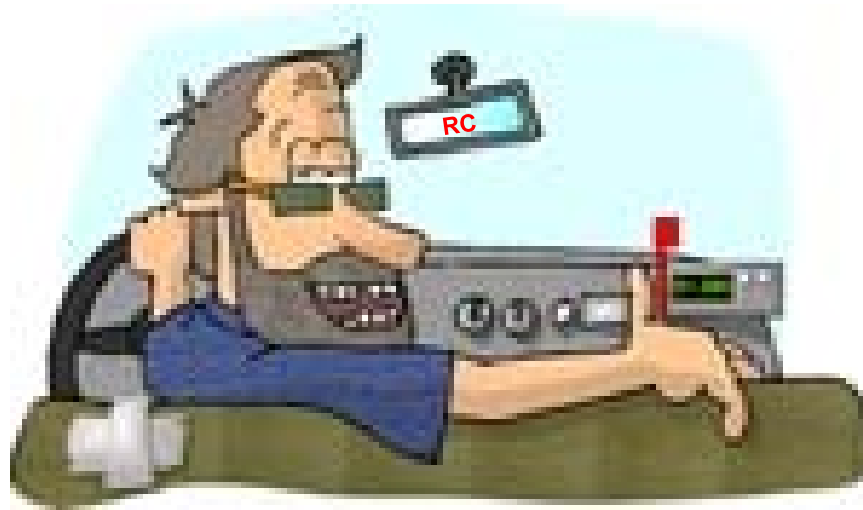
- HLL's
 - Abstraction
- Interactive Development
 - Turns Per Day
- Integrated Environments
 - Reuse

Don't Look Back



- The best is yet to come...

Don't Look Back



- The best is yet to come...